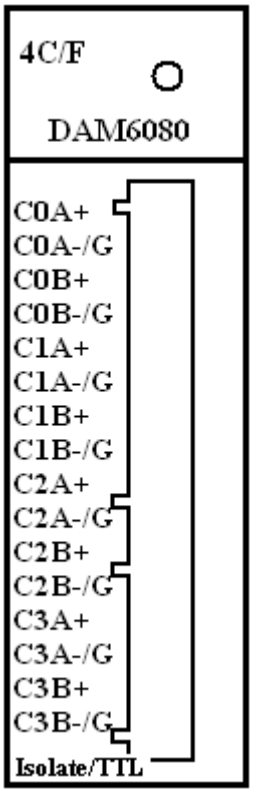
DAM6080

User's Manual

Beijing ART Technology Development Co., Ltd.

DAM6080

◆ Terminal Distribution



◆ Feature

4-channel Counter/Frequency Module

- 4-channel 32-bit counter
- Input signal can be set to isolated or non-isolated (jumper selectable)
- Input Frequency:

  1~1000HZ max (frequency mode)

  5000HZ max (counter mode)
- Mode: count (double-pulse, single-pulse) frequency
- Isolation Voltage: 2500Vrms
- Input Voltage:

  Isolation: logic level 0: +1V (MAX)

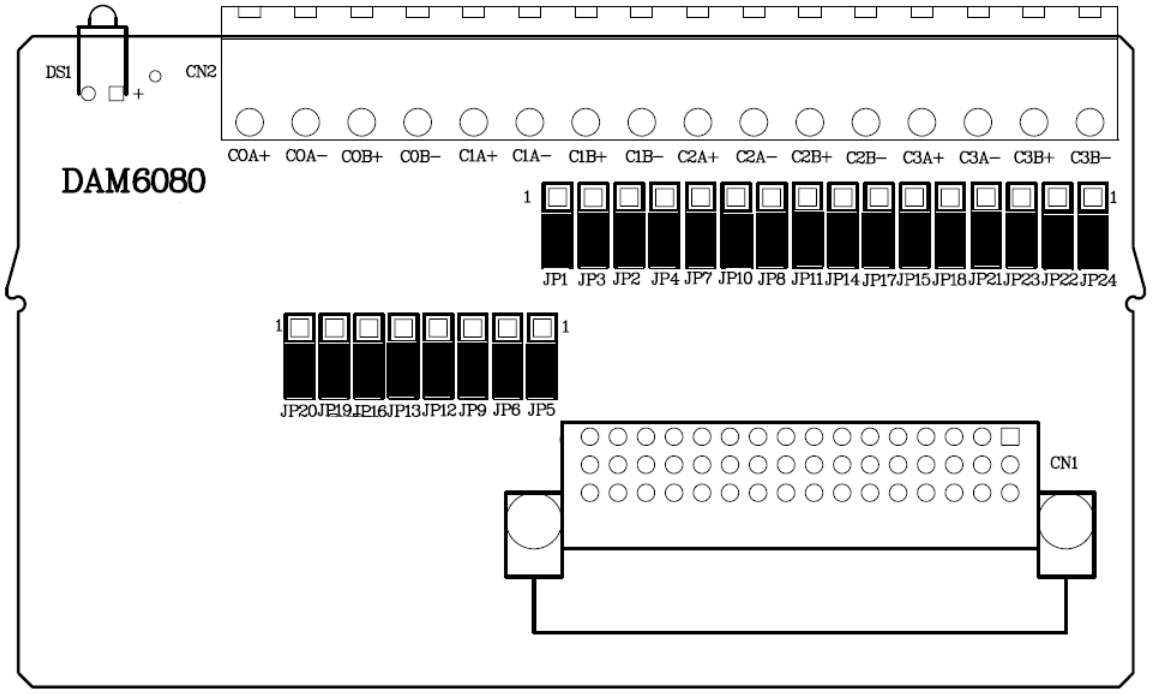
  logic level 1: + 3.5V~ 30V

  Non-isolated: logic level 0: 0V ~ 0.8V

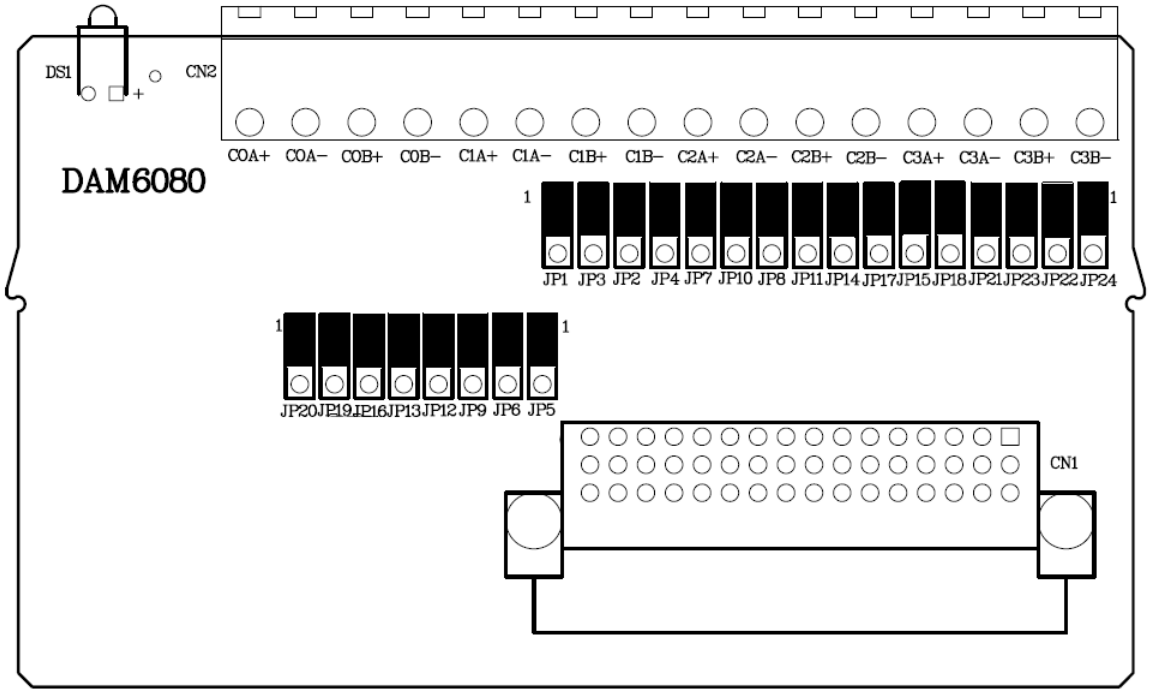
  logic level 1: 2.3V~ 5V
- Programmable Digital Noise Filter: 8~65000μsec
- Power Consumption: 1W (+5VDC power)

◆ Internal Circuit Jumper Selection

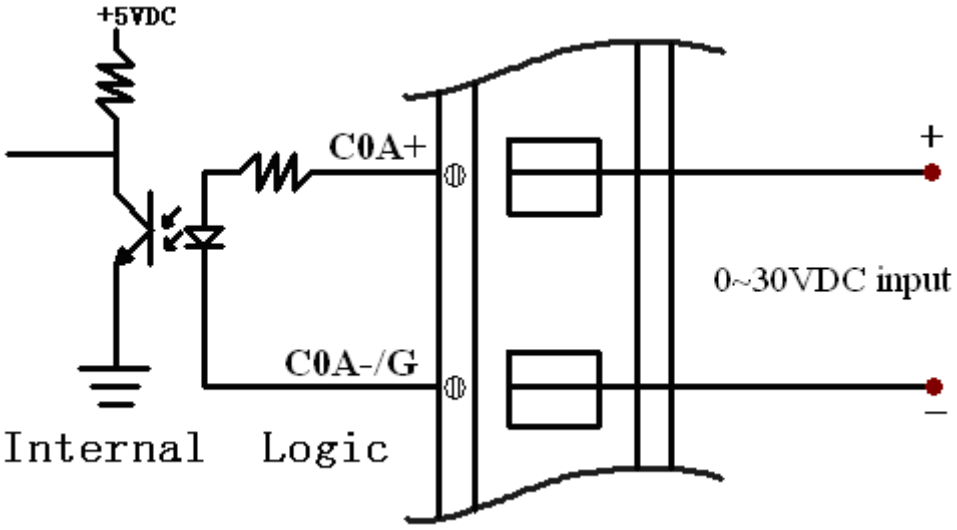
Isolation Selection



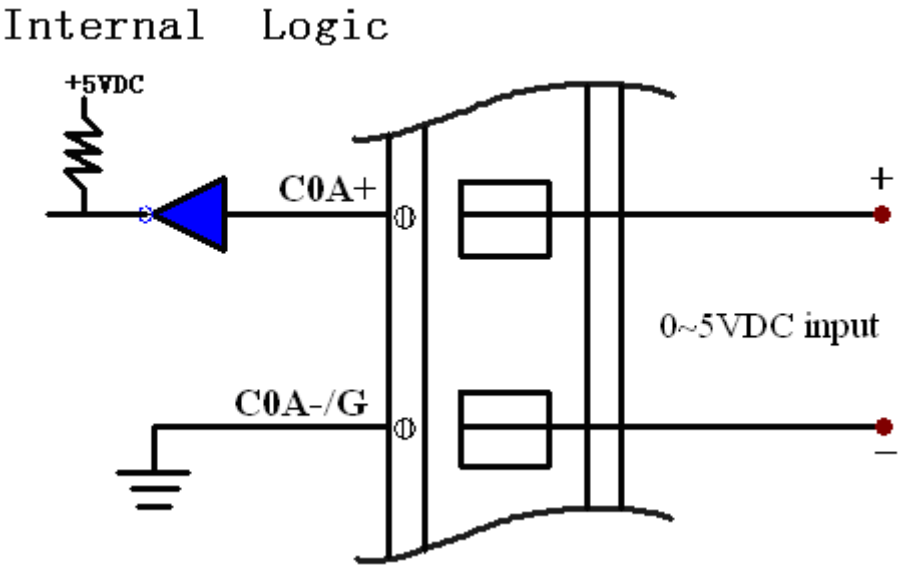
Non-isolated Selection



◆ Wiring



Isolation Wiring (B signal is the same as A signal)



Non-isolated Wiring (B signal is the same as A signal)

There are three working mode (software selection), including the double-pulse count mode, single-pulse count mode, and the frequency mode.

1. Double-pulse Count Mode

The frequency of the count mode up to 5000Hz, the voltage range shown as the parameters. When in adding count mode, only connect with A signal, in reduction count, only connect with B signal. When there are both A signal and B signal, the encoder output frequency of the A and B are the same, so the module does not count. If connect with the signal generator, the frequency of the two signal generators are different, so the count value is the difference of A frequency and the B frequency.

2. Single-pulse Count Mode

The frequency of the count mode up to 5000Hz, the voltage range shown as the parameters. B signal control the count direction. There are two logic level of B signal, logic level 0 (adding count), and logic level 1(reduction count).

Note: in the isolated state and non-isolated state, the voltage of the B signal is different.

3. Frequency Mode

In this mode, only connect A signal, the frequency range is 1~1000Hz.

◆ Address Configuration Table

Address（A8~A1）	Operating	Direction
x00	D[1:0]counter0 mode control word D[3:2] counter1 mode control word D[5:4] counter2 mode control word D[7:6] counter3 mode control word Mode control word direction 00: single-pulse mode 01: double-pulse mode 10: frequency mode	Can be read back
x01	D[0] effective, channel 0 measurement frequency timer length = 0 measurement frequency timer 10ms = 1 measurement frequency timer 1s	Can be read back
x02	D[0] effective, channel 1 measurement frequency timer length = 0 measurement frequency timer 10ms = 1 measurement frequency timer 1s	Can be read back
x03	D[0] effective, channel 2 measurement frequency timer length = 0 measurement frequency timer 10ms = 1 measurement frequency timer 1s	Can be read back
x04	D[0] effective, channel 3 measurement frequency timer length = 0 measurement frequency timer 10ms = 1 measurement frequency timer 1s	Can be read back
x05	Counter 0 initial value setting CNT0[31:0]	Can be read back
x06	Counter 0 initial value setting CNT0[23:16]	Can be read back
x07	Counter 0 initial value setting CNT0[15:8]	Can be read back
x08	Counter 0 initial value setting CNT0[7:0]	Can be read back
x09	Counter 1 initial value setting CNT1[31:0]	Can be read back
x0A	Counter 1 initial value setting CNT1[23:16]	Can be read back
x0B	Counter 1 initial value setting CNT1[15:8]	Can be read back
x0C	Counter 1 initial value setting CNT1[7:0]	Can be read back
x0D	Counter2 initial value setting CNT2[31:0]	Can be read back
x0E	Counter 2 initial value setting CNT2[23:16]	Can be read back
x0F	Counter 2 initial value setting CNT2[15:8]	Can be read back
x10	Counter 2 initial value setting CNT2[7:0]	Can be read back
x11	Counter 3 initial value setting CNT3[31:0]	Can be read back
x12	Counter 3 initial value setting CNT3[23:16]	Can be read back
x13	Counter 3 initial value setting CNT3[15:8]	Can be read back
x14	Counter 3 initial value setting CNT3[7:0]	Can be read back
x15	Counter 0 upper limit setting CNT0[15:0]CNT0_H_VAL[31:0]	Can be read back
x16	Counter 0 upper limit setting	Can be read back

	CNT0_H_VAL [23:16]	
x17	Counter 0 upper limit setting CNT0_H_VAL [15:8]	Can be read back
x18	Counter 0 upper limit setting CNT0_H_VAL [7:0]	Can be read back
x19	Counter 1 upper limit setting CNT1_H_VAL[31:0]	Can be read back
x1A	Counter 1 upper limit setting CNT1_H_VAL [23:16]	Can be read back
x1B	Counter 1 upper limit setting CNT1_H_VAL [15:8]	Can be read back
x1C	Counter 1 upper limit setting CNT1_H_VAL [7:0]	Can be read back
x1D	Counter 2 upper limit setting CNT2_H_VAL[31:0]	Can be read back
x1E	Counter 2 upper limit setting CNT2_H_VAL [23:16]	Can be read back
x1F	Counter 2 upper limit setting CNT2_H_VAL [15:8]	Can be read back
x20	Counter 2 upper limit setting CNT2_H_VAL [7:0]	Can be read back
x21	Counter 3 upper limit setting CNT3_H_VAL[31:0]	Can be read back
x22	Counter 3 upper limit setting CNT3_H_VAL [23:16]	Can be read back
x23	Counter 3 upper limit setting CNT3_H_VAL [15:8]	Can be read back
x24	Counter 3 upper limit setting CNT3_H_VAL [7:0]	Can be read back
x25	Counter 0 lower limit setting CNT0_L_VAL[31:0]	Can be read back
x26	Counter 0 lower limit setting CNT0_ L _VAL [23:16]	Can be read back
x27	Counter 0 lower limit setting CNT0_ L _VAL [15:8]	Can be read back
x28	Counter 0 lower limit setting CNT0_ L _VAL [7:0]	Can be read back
x29	Counter 1 lower limit setting CNT1_L_VAL[31:0]	Can be read back
x2A	Counter 1 lower limit setting CNT1_ L _VAL [23:16]	Can be read back
x2B	Counter 1 lower limit setting CNT1_ L _VAL [15:8]	Can be read back
x2C	Counter 1 lower limit setting CNT1_ L _VAL [7:0]	Can be read back
x2D	Counter 2 lower limit setting CNT2_L_VAL[31:0]	Can be read back
x2E	Counter 2 lower limit setting CNT2_ L _VAL [23:16]	Can be read back
x2F	Counter 2 lower limit setting CNT2_ L _VAL [15:8]	Can be read back
x30	Counter 2 lower limit setting CNT2_ L _VAL [7:0]	Can be read back
x31	Counter 3 lower limit setting CNT3_L_VAL[31:0]	Can be read back
x32	Counter 3 lower limit setting CNT3_ L _VAL [23:16]	Can be read back
x33	Counter 3 lower limit setting	Can be read back

	CNT3_ L _VAL [15:8]	
x34	Counter 3 lower limit setting CNT3_ L _VAL [7:0]	Can be read back
x35		D[7:0] The current count value of Counter 0, COUNT[31:24]
x36		D[7:0] The current count value of Counter 0, COUNT[23:16]
x37	Write address, clear interrupt	D[7:0] The current count value of Counter 0, COUNT[15:8]
x38	Counter reset control D [0]: counter 0 reset control D [1]: counter 1 reset control D [2]: counter 2 reset control D [3]: counter 3 reset control Write 1 to reset the corresponding counter	D[7:0] The current count value of Counter 0, COUNT[7:0]
x39	D [0]: counter 0 start-stop control 1: start, 0: stop	D[7:0] The current count value of Counter 1, COUNT[31:24]
x3A	D [0]: counter 1 start-stop control 1: start, 0: stop	D[7:0] The current count value of Counter 1, COUNT[23:16]
x3B	D [0]: counter 2 start-stop control 1: start, 0: stop	D[7:0] The current count value of Counter 1, COUNT[15:8]
x3C	D [0]: counter 3 start-stop control 1: start, 0: stop	D[7:0] The current count value of Counter 1, COUNT[7:0]
x3D		D[7:0] The current count value of Counter 2, COUNT[31:24]
x3E		D[7:0] The current count value of Counter 2, COUNT[23:16]
x3F		D[7:0] The current count value of Counter 2, COUNT[15:8]
x40		D[7:0] The current count value of Counter 2, COUNT[7:0]
x41		D[7:0] The current count value of Counter 3, COUNT[31:24]
x42		D[7:0] The current count value of Counter 3, COUNT[23:16]
x43		D[7:0] The current count value of Counter 3, COUNT[15:8]
x44		D[7:0] The current count value of Counter 3, COUNT[7:0]
x45		Counter 0 interrupt status D[0]:=1 overflow , =0 no overflow D[1]:=1 underflow, =0 no underflow D[2]:=1 upper limit, =0 no Upper limit

		D[3]:=1 lower limit, =0 no lower limit
x46		Counter 1 interrupt status D[0]:=1 overflow , =0 no overflow D[1]:=1 underflow, =0 no underflow D[2]:=1 upper limit, =0 no Upper limit D[3]:=1 lower limit, =0 no lower limit
x47		Counter 2 interrupt status D[0]:=1 overflow , =0 no overflow D[1]:=1 underflow, =0 no underflow D[2]:=1 upper limit, =0 no Upper limit D[3]:=1 lower limit, =0 no lower limit
x48		Counter 3 interrupt status D[0]:=1 overflow , =0 no overflow D[1]:=1 underflow, =0 no underflow D[2]:=1 upper limit, =0 no Upper limit D[3]:=1 lower limit, =0 no lower limit
x49	Counter filter coefficient high 8-bit setting	Can be read back (unit: us)
x4A	Counter filter coefficient low 8-bit setting	Can be read back (unit: us)
X4B		All channel counters latch
b1XXXXXXX		D [7:0] read back the ID Fixed 80H

Double-pulse Count: count the difference between A and B.

Single-pulse Count: count the rising edge and falling edge, B control the direction, 1: adding count, 0: reduction count.

Frequency Measurement: pulse format within a given time.